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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/811,032	03/26/2004	Alexander Levin	42P18580	9556

8791 7590 10/14/2005

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EXAMINER	
TRAN, ANH Q	
ART UNIT	**PAPER NUMBER**
2819	

DATE MAILED: 10/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No. 10/811,032	Applicant(s) LEVIN, ALEXANDER
	Examiner Anh Q. Tran	Art Unit 2819

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 August 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure\Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-5, 9-15, 19-30 are rejected under 35 U.S.C. 102(e) as being anticipated by Rokhsaz (6,566,950).

Rokhsaz shows:

1. A predriver circuit comprising:

a pull-up circuit (138, 142, Fig. 6) having at least one pull-up device of a first device type (NMOS); and

a pull-down circuit (140, 144) including at least one pull-down device of the first device type (the source of NMOS transistors 140 & 140 are directly connected to ground) having a source coupled to ground (ground), the pull-up circuit and the pull-down circuit to charge an output node and a complement output node in opposite directions to generate a differential predriver signal pair.

2. The predriver circuit of claim 1, wherein the pull-up device is cross- coupled to the pull-down device (transistors 142 & 140 is cross-coupled and transistors 138 & 144 is cross-coupled).

3. The predriver circuit of claim 1, wherein the pull-up device and the pull- down device comprise NMOS devices (col. 7, lines 40-55).

4. The predriver circuit of claim 1, wherein the pull-up circuit comprises:

a first pull-up device (142) having a gate coupled to a data input signal, a drain coupled to a power supply and a source coupled to the output node; and

a second pull-up device (138) having a gate coupled to a complement input signal, a drain coupled to the power supply and a source coupled to the complement output node.

5. The predriver circuit of claim 1, wherein the pull-down circuit comprises: a first pull-down device (140) having a gate coupled to a complement input signal, a drain coupled to the output node and a source coupled to ground; and a second pull-down device (144) having a gate coupled to a data input signal, a drain coupled to the complement output node and a source coupled to ground.

9. The predriver circuit of claim 2, further comprising:

a first pull-up device (142) cross-coupled to a first pull-down device to receive a data input signal and to charge the output node and the complement output node in opposite directions; and

a second pull-up device (138) cross-coupled to a second pull-down device to receive a complement data input signal and to charge the output node and the complement output node in opposite directions to generate the differential predriver signal pair.

10. The predriver circuit of claim 1, wherein the first and second pull-up devices comprise NMOS devices and the first and second pull-down devices comprise NMOS devices (all NMOS transistors).

11-15, 19-20, 26-30. the limitations are rejected as above claims.

21. An electronic system (Fig. 1) comprising:

a printed wiring board (col. 3, line 45) on which a serial bus (14) is formed, an integrated circuit (IC) chip package (12) being operatively installed on the board to communicate using the serial bus, the package having an IC chip that includes a logic function section and an I/0 section (col. 3, lines 5-21) as an interface between the logic function section and the serial bus, the I/0 section having an output driver (amplifier circuit 32) in which a pre- driver (the rest of the limitations are rejected as above claims 1-5, and 9-10).

22-25 wherein the logic function section is microprocessor, memory controller, bus bridge, or an I/O controller (the electronic device 12 can be any device that manipulates signals, analogs or digital, based on operational instructions, col. 3, lines 5-21).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

> invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 6-8, 16-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rokhsaz (6,566,950) in view of Bass (6,407,590).

Rokhsaz discloses the claimed invention except for a first NMOS transistor having a gate and a drain connected to the output node and a source coupled to ground, a second NMOS transistor having a gate and a drain connected to the complement output node and a source coupled to ground.

Bass shows a first NMOS transistor (30, Fig. 1) having a gate and a drain connected to the output node (40) and a source coupled to ground (VSS), a second NMOS transistor (32) having a gate and a drain connected to the complement output node (38) and a source coupled to ground.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the output node and the complement output node of Rokhsaz with a first NMOS transistor having a gate and a drain connected to the output node and a source coupled to ground, a second NMOS transistor having a gate and a drain connected to the complement output node and a source coupled to ground of Bass, in order to clamp the differential output swing from becoming too large.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh Q. Tran whose telephone number is 571-272-1813. The examiner can normally be reached on M-F (8:00-5:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal can be reached on 571-272-1769. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

10/4/05

ANH Q. TRAN
PRIMARY EXAMINER

10/4/05